STANDARDS AND INFORMATION DOCUMENTS

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(revision AES-R8-2015)

AES standards project report - Synchronisation of digital audio over wide areas

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Abstract

When several digital signals are combined in a mixing desk or other equipment, they must share the same sample clock. If all the signals originate within the same studio, it is sufficient to synchronise all the equipment within that studio. With the introduction of transmission of signals in digital form between studios, the problem takes on a new dimension.

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Contents

Foreword

This foreword is not part of the *AES standards project report - Synchronisation of digital audio over wide areas*, AES-R8.

This content of this document was developed within Task Group SC-02-05-D, whose members included: R. Caine, C. Chambers, R. Foss, C. Gaunt, J. Grant, S. Harris, H. Jahne, P. Johansson, M. Karagisian, B. Klinkradt, C. Meyer, S. Scott, J. Strawn, T. Thaler, C. Travis, R. van der Hilst. Final development was handled by working group SC-02-02.

John Grant
Chair, AESSC SC-02-02 Working Group on Digital Input/Output Interfacing, 2007-11-22

Foreword to 2015 revision

In order to make the document more accessible, the background material has been extended to explain more of the details. More reference has been made to various technologies that are in use. Re-arrangements have been made to group the recommendations better, and relate them to the various connection scenarios. More guidance to current use has been provided. Additionally, references to telecommunication standards have been provided, as additional reading material for the interested, as they discuss similar long-distance connections. Finally, a new clause has been added to discuss the synchronization side of monitoring, providing some guidance on monitoring that may be needed for good operation.

The content of this document was developed by M. Danielson, J. Grant, and K. Gross. Final development was handled by working group SC-02-02.

John Grant
Chair, SC-02-02 Working Group on Digital Input/Output Interfacing, 2015-08

Foreword to 2020 revision

This revision includes minor changes to remove insensitive terms.

J. Grant
Chair, SC-02-02 Working Group on Digital Input/Output Interfacing, 2020-11-27

Note on normative language

In AES standards documents, sentences containing the word “shall” are requirements for compliance with the document. Sentences containing the verb “should” are strong suggestions (recommendations). Sentences giving permission use the verb “may”. Sentences expressing a possibility use the verb “can”.

AES standards project report - Synchronisation of digital audio over wide areas

1 Scope

This document is intended to provide guidance on synchronisation issues to implementers of systems in which an audio signal originated in digital form in one location is transmitted over a digital network to another location.

2 Background

2.1 Basic synchronisation

In order for the receiver to recover all the data from a transmitter, the receiver needs to be synchronised to the same clock as the transmitter. The reason is that even a fractional offset between two clocks will over time result in having too many or too few samples, and require a re-alignment, a slip, which is audible, thus affecting the quality of the transmission.

A typical device has a core clock, which is either free-running or steered to match the frequency of one of its input references, be it a signal or a clock input. The steering is done using a Phase-Locked Loop (PLL), which will steer the oscillator's frequency and phase to match the reference. The PLL also filters jitter, but follows the reference in its long-term phase and frequency. Digital PLLs with the control element implemented in software are able to implement narrower bandwidth and higher order PLLs and thus able to filter out jitter much more effectively than analogue PLLs. For some applications an analogue PLL is sufficient.

The simplest scheme is where the transmitting device provides the synchronisation signal to the receiving device embedded in a signal such as AES3. In this scenario the synchronisation signal may also be provided by a separate word clock, which has been the case for older digital interfaces, but is regularly seen in interfacing digital-to-analog converter (DAC) chips.

A more complex situation exists in a studio where there are multiple sources, and where the sample-rates need to be coordinated so that digital mixing can be performed. In such cases all the sources (such as analog-to-digital converters (ADCs) on inputs and also digital play-back units) are synchronised to a common clock source. The AES11 standard details many aspects of this, including a Digital Audio Reference Signal (DARS) as a variant of an AES3 signal, but also the traditional Word Clock signal can provide the same synchronisation. AES11 is however limited to a local area, for example a studio or studio complex.

2.2 Re-alignment of received samples

In a receiver, the first part of the receiver always uses a clock recovered from the received bit-stream. If the receiving device is locked to the incoming stream, this recovered clock can also be used for further processing provided it has low enough jitter. However, if the receiving device is synchronised from another source, even one that is frequency-locked to the same reference as the source of the incoming stream, the phase of the input and the phase of the local clock cannot be assumed to match up. For this purpose a First-In-First-Out (FIFO) buffer is used. The FIFO is written using the recovered clock and read using the device's internal clock. Such a FIFO is often implemented in the form of a circular buffer with separate read and write pointers.