Multicore SOCs: Performance, Analysis and Optimization

John Whitecar
DSP Concepts
Automotive Industry Trends

- Systems are getting more complicated
- Needs agility to reduce development time
- Audio processing moving to the head unit
- OEMs want to be involved
- SOCs are getting more powerful
  - Many are multicore
- De-aggregation of systems
Growing Complexity of Systems

• Playback
• Hands free communication
• Voice user interface
• Pedestrian warning / eSound
• Active noise cancellation
• In car communication
• 3D audio
• Sound sets / presets / VIP tunings
• Etc.
Audio Processing Moving to Main CPU

Offers significant advantages:
• Cost savings
• Reduced complexity
• Simplified architecture
• Easier path for software upgrades

This trend has started and is inevitable. PC sound cards went through this same change about 15 years ago
Hardware Cost Savings

Traditional Architecture

Upcoming Architecture

Cost savings:
- $10 DSP
- $4 Micro
- $3 RAM
- $1 Flash
- -$3 Audio I/F
- $15 Total
Growing Power of SOCs

Features
• Multiple application processors
• Dedicated audio DSPs
• Audio peripherals (serial ports, sample rate converters, etc.)

Example SOCs
• Intel Skylake / Apollo Lake
  • 4 x86 cores @ 1.9 GHz
  • 2 x HiFi 3 DSPs @ 300 MHz
• Renesas R-Car
  • 4 x ARM Cortex-A57 @ 2.4 GHz
  • 1 x HiFi @ 500 MHz
• TI Jacinto 6
  • 2 x ARM Cortex-A15 @ 1.5 GHz
  • 2 x C66x DSPs @ 600 MHz
Multicore SOC memory architecture
Benchmarking with Audio Weaver®

- Cross platform
- Highly optimized code
- Used in automotive
- Built in profiling capabilities
- Supports multicore SOCs
Audio System to Benchmark

- Stereo or 7.1 sources
- 4 announcement channels
- Fader / balance / volume / tone
- Multiband compressors
- Loudness compensation
- Upmix to 7.1 (8 channel)
- Equalizers for 8 spatial zones
- IIR crossovers to generate 21 speaker channels
- Independent limiters per output channel
3 Test Cases

• 1. **Low memory.** EQs were implemented as eight-stage biquad filters (16\textsuperscript{th} order). Total data memory usage was 365 kbytes.

• 2. **Medium memory.** EQs were implemented as 4096-point FIR filters using an efficient FFT-based algorithm. Total data memory usage was 1188 kbytes.

• 3. **High memory.** EQs were implemented as 16384-point FIR filters using an efficient FFT-based algorithm. Total data memory usage was 2724 Kbytes.

This includes all memory for parameters, state variables, and buffers. The executable code required another approximately 600 kbytes which is not included as part of the data memory numbers.
# Single Core Performance

<table>
<thead>
<tr>
<th>Configuration</th>
<th>SoC-1</th>
<th>SoC-2</th>
<th>SoC-3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low memory</td>
<td>21%</td>
<td>28%</td>
<td>56%</td>
</tr>
<tr>
<td>Medium memory</td>
<td>29%</td>
<td>38%</td>
<td>95%</td>
</tr>
<tr>
<td>High memory</td>
<td>52%</td>
<td>N/A – Memory BW limit</td>
<td>N/A – CPU throughput limit</td>
</tr>
</tbody>
</table>
Consistent Processing Load

Audio priority has to be correctly set.
CPU load is consistent
We can see clock scaling going on
This is a bare metal Linux optimized for an infotainment system

9/20/2017
Multiple tasks on HLOS

PC
High memory system.
Single instance
Multicore Performance

SoC-1. Low Memory

1 Core Loading  2 Core Loading  3 Core Loading  4 Core Loading

Core 1  Core 2  Core 3  Core 4

SoC-2. Low Memory

1 Core Loading  2 Core Loading  3 Core Loading  4 Core Loading

Core 1  Core 2  Core 3  Core 4
High Memory

SoC-1. High Memory

- Core 1
- Core 2
- Core 3
- Core 4

1 Core Loading
2 Core Loading
3 Core Loading
4 Core Loading
Conclusions

• Automotive systems increasing complexity
• Audio processing moving to headunit SOCs
• Multicore SOCs are capable of running audio concurrently
• Priority must be given to audio
• L2 Cache size/architecture important to consider for realtime performance across cores
Thank You!